

FIG. 1

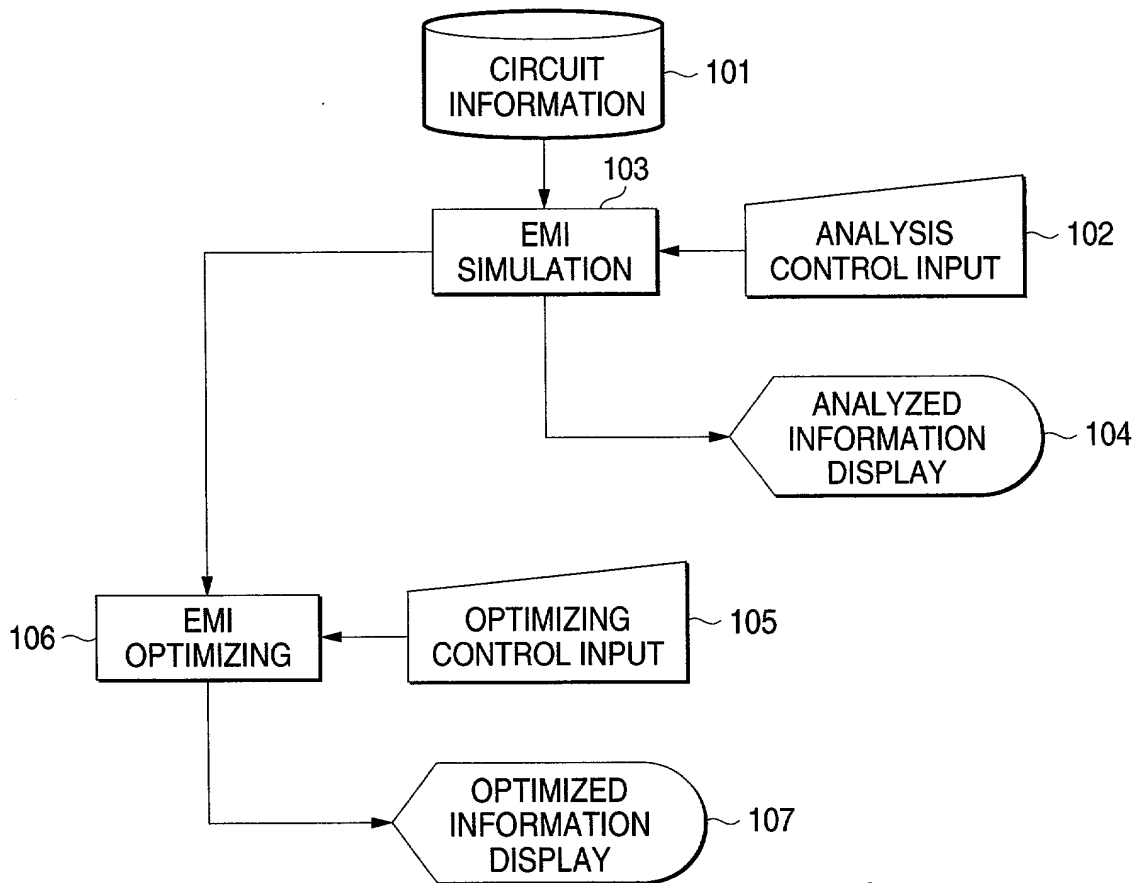


FIG. 2

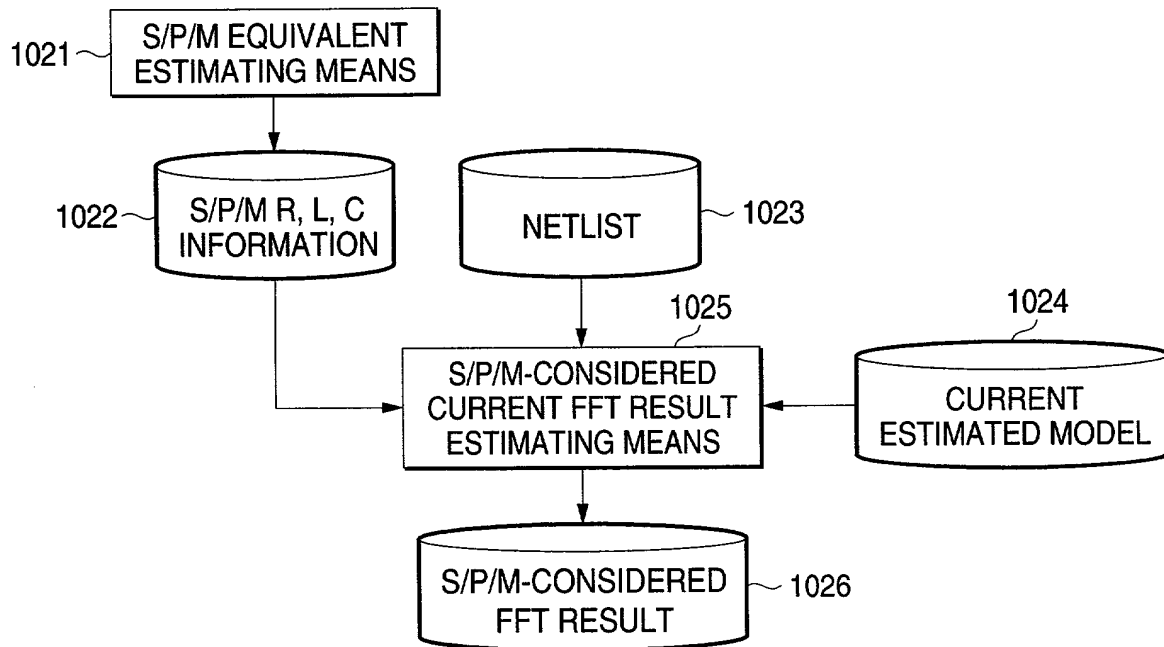


FIG. 3

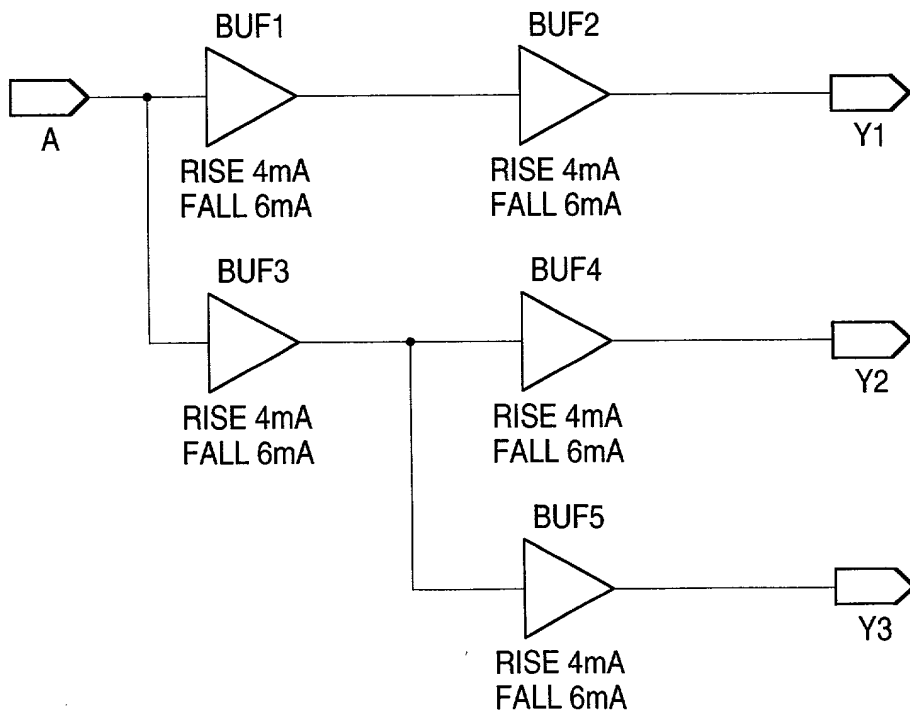


FIG. 4

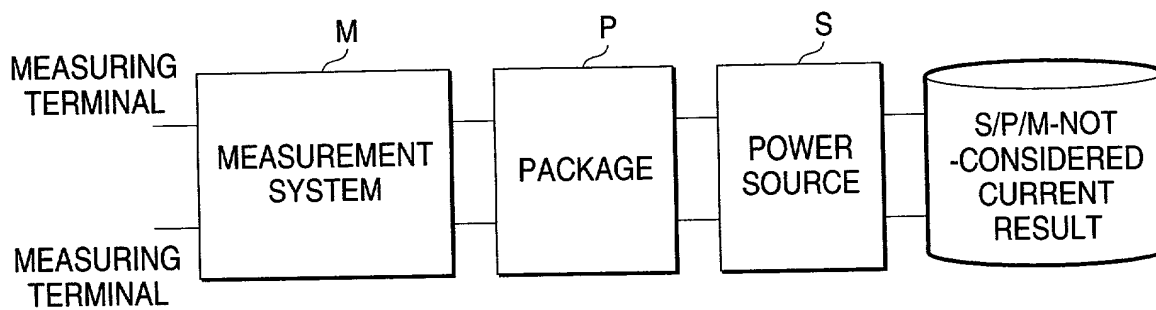
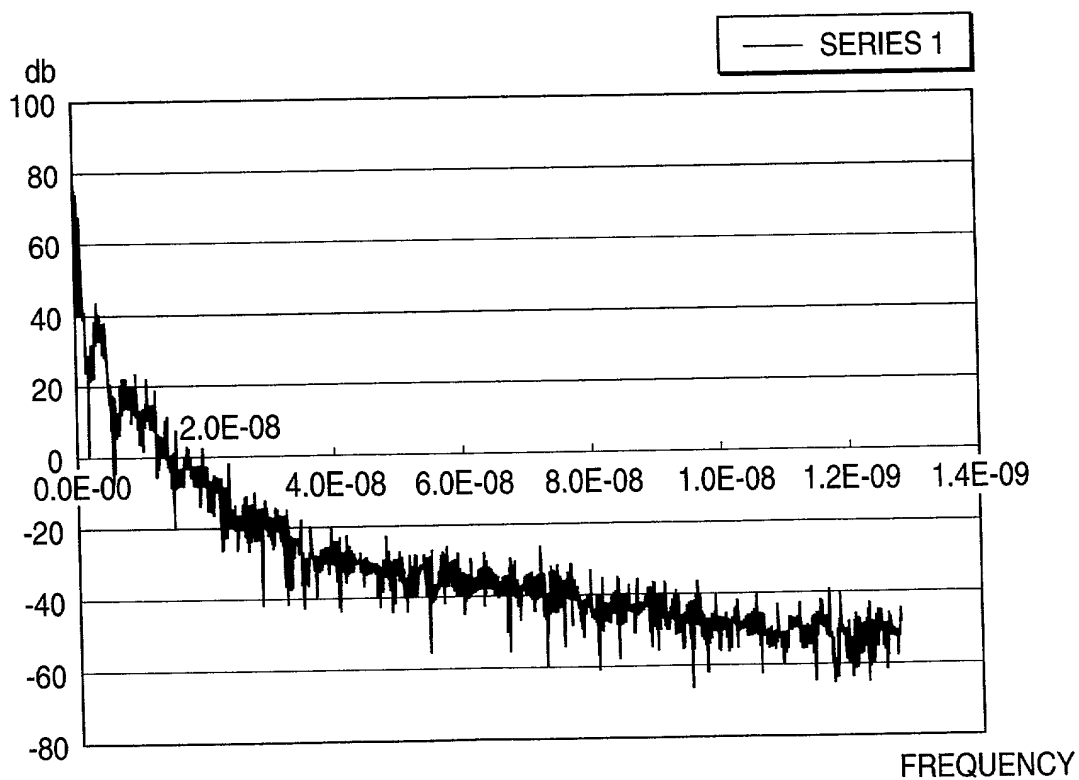
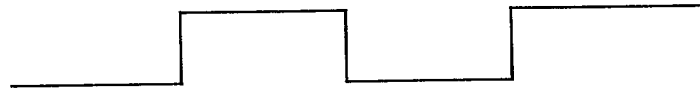
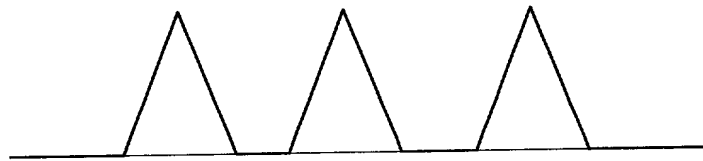
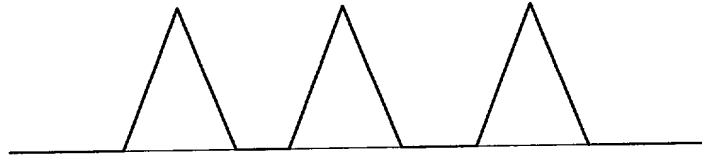


FIG. 5



*FIG. 6 (a)**FIG. 6 (b)*

LOGICAL CHANGE

*FIG. 6 (c)*ESTIMATED POWER SOURCE  
CURRENT AT SMALL  
DECOUPLING CAPACITANCE*FIG. 6 (d)*ESTIMATED POWER SOURCE  
CURRENT AT LARGE  
DECOUPLING CAPACITANCE*FIG. 7 (a)**FIG. 7 (b)*

LOGICAL CHANGE

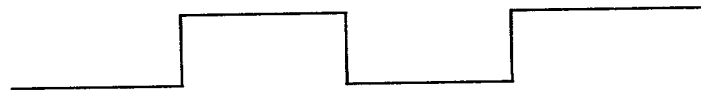
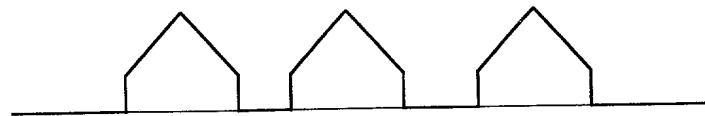
*FIG. 7 (c)*ESTIMATED POWER SOURCE  
CURRENT AT SMALL  
DECOUPLING CAPACITANCE*FIG. 7 (d)*ESTIMATED POWER SOURCE  
CURRENT AT LARGE  
DECOUPLING CAPACITANCE

FIG. 8

TIMING [ ns ]	POWER SOURCE CURRENT VALUE [ mA ]
0	0
95	20
100	50
105	20
195	30
200	70
205	30
295	20
300	50
305	20
395	30
400	70
405	30
495	20
500	30
505	20

801 802

FIG. 9

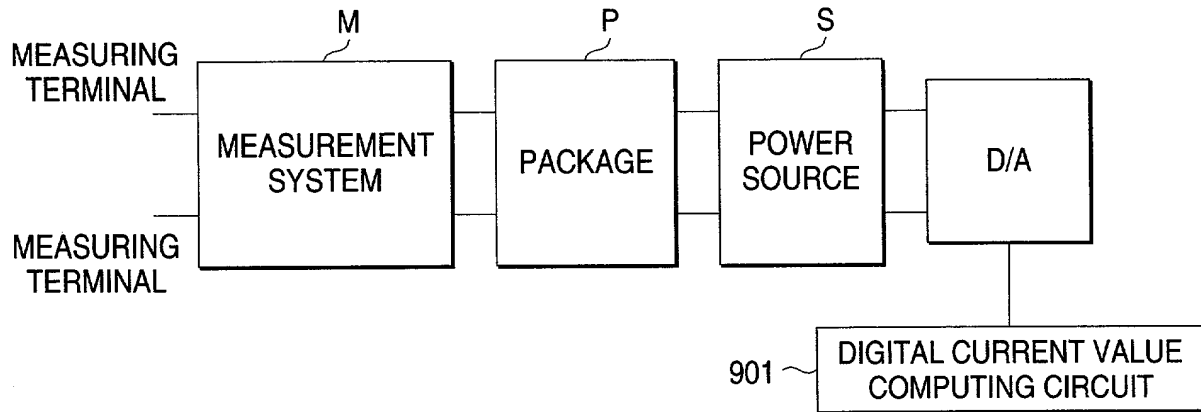


FIG. 10

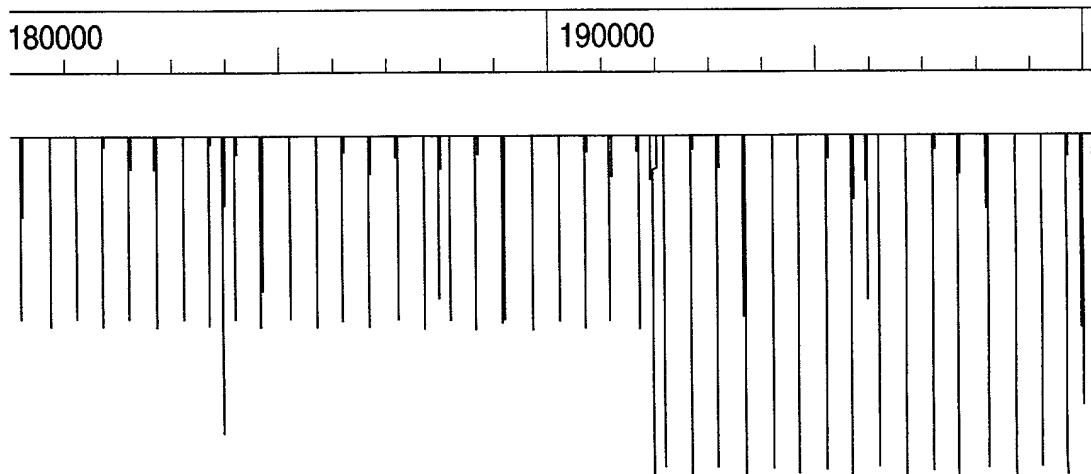


FIG. 11

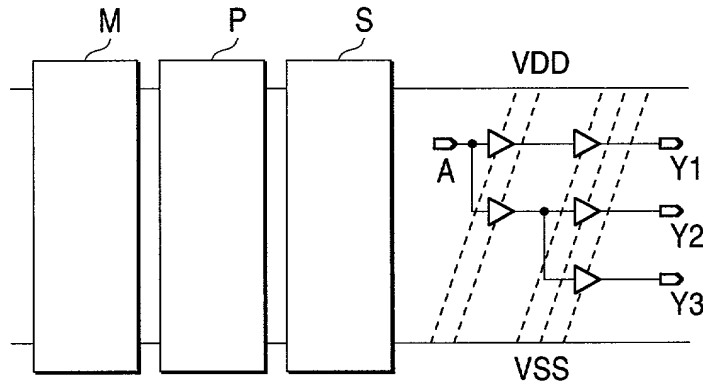


FIG. 12

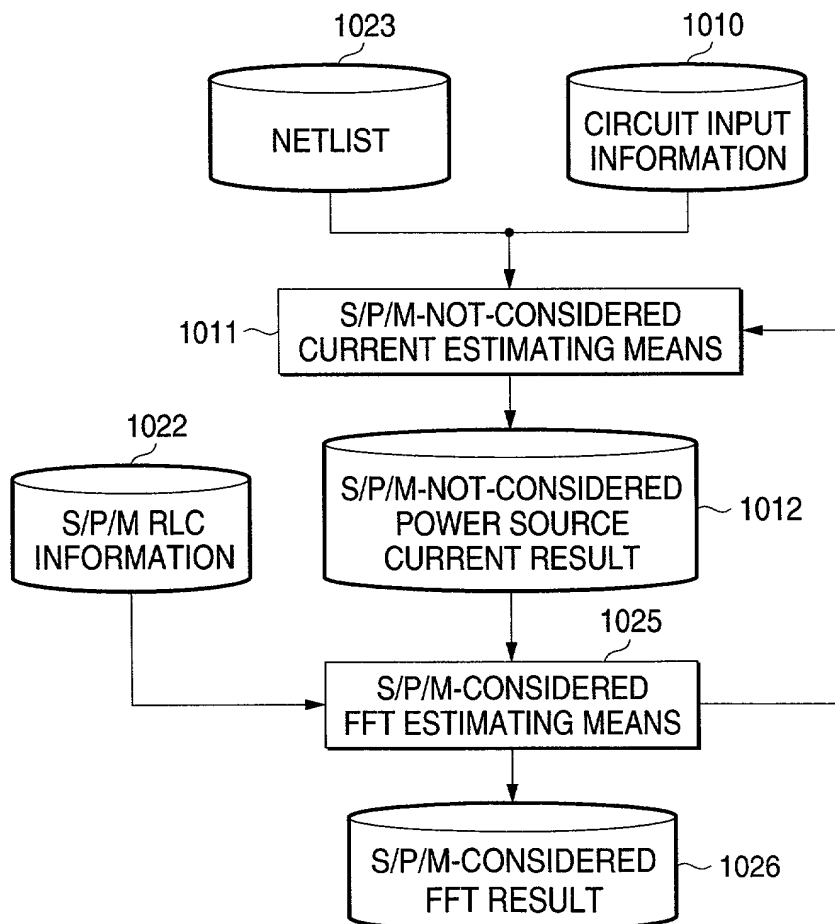


FIG. 13

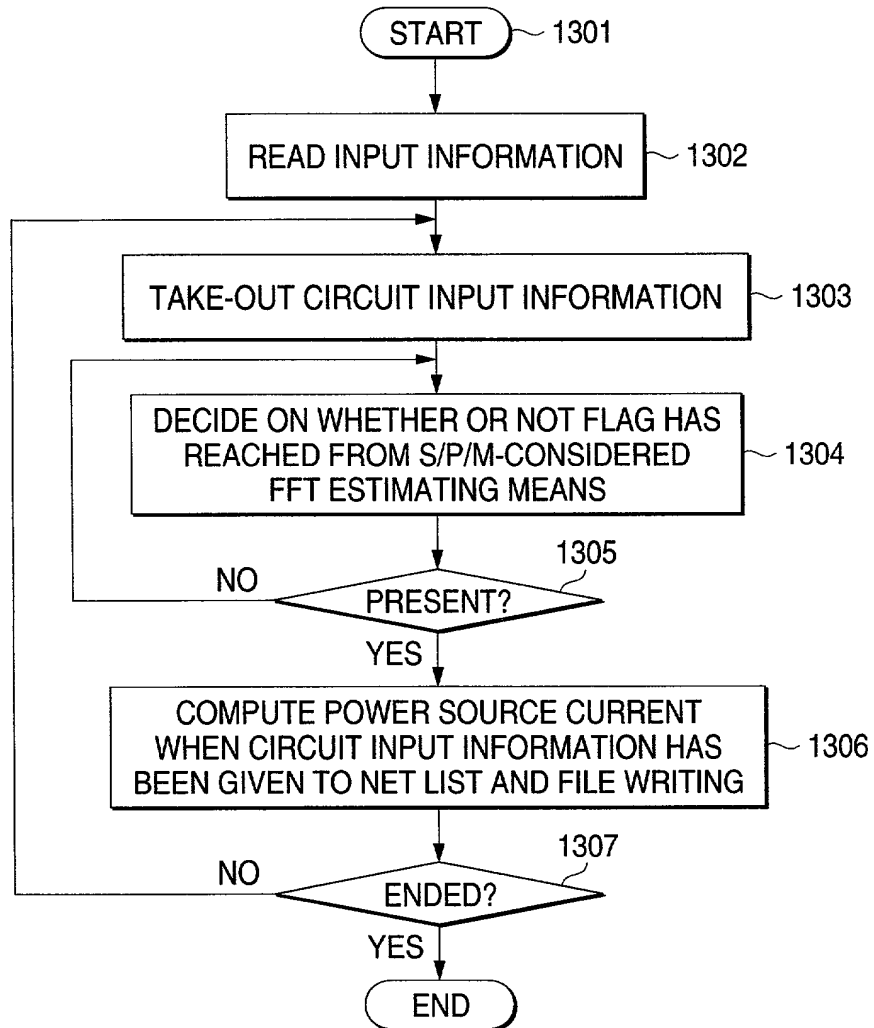




FIG. 14

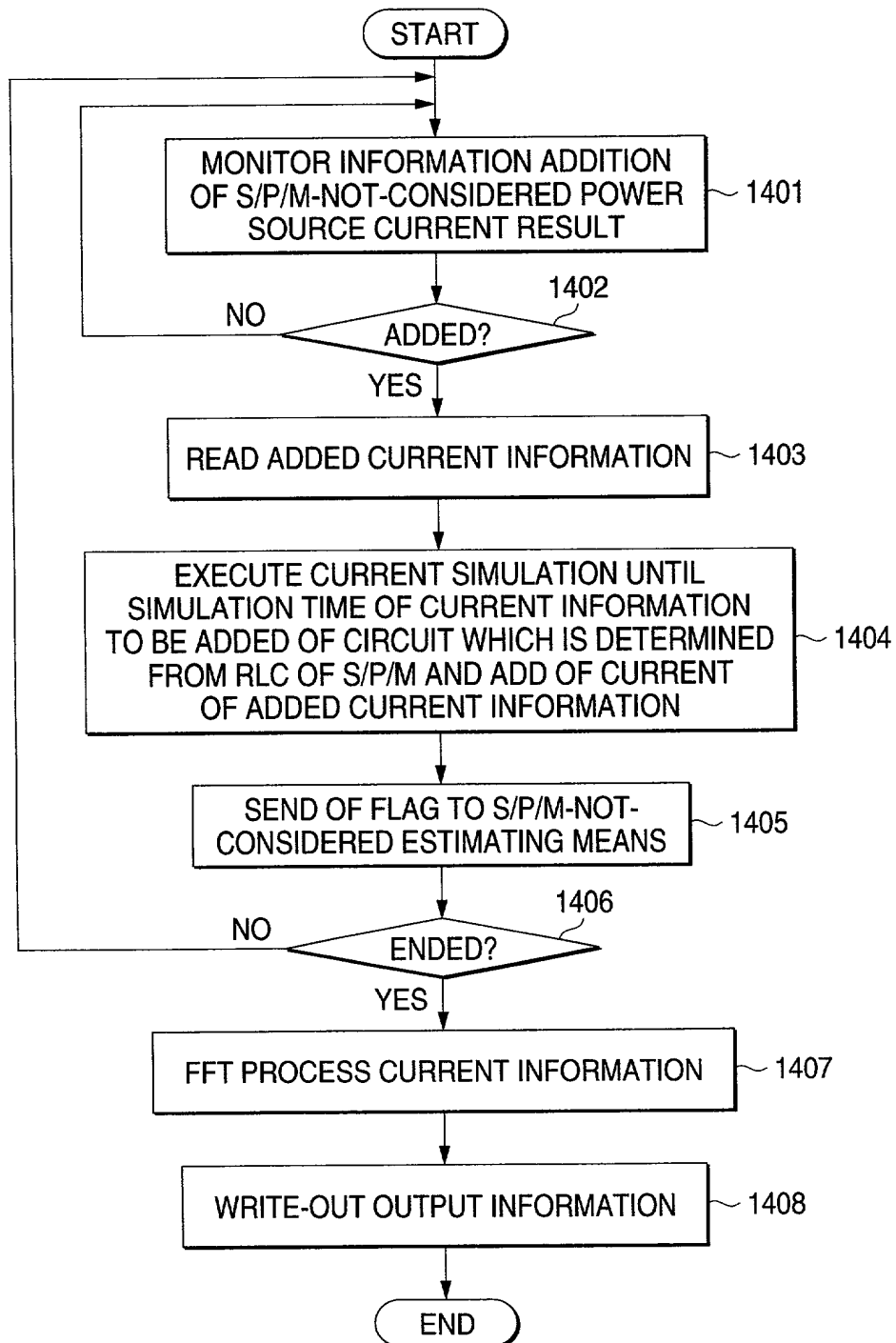


FIG. 15

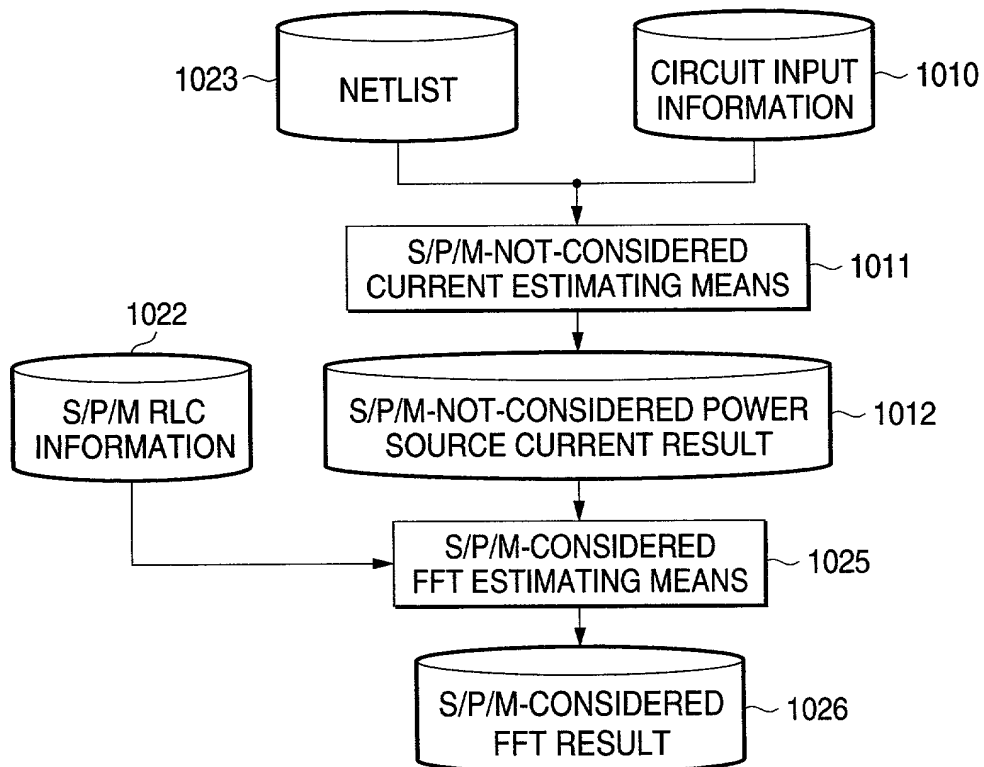


FIG. 16

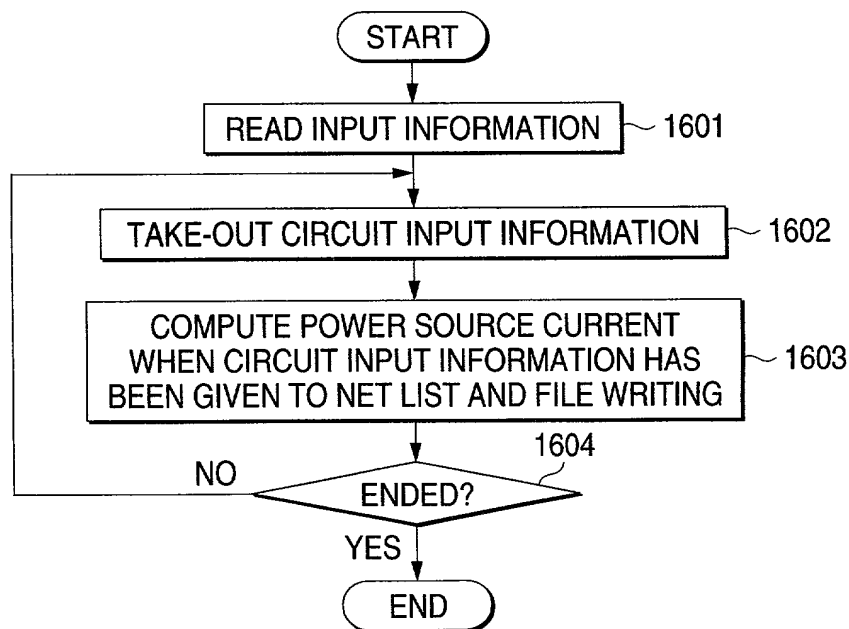


FIG. 17

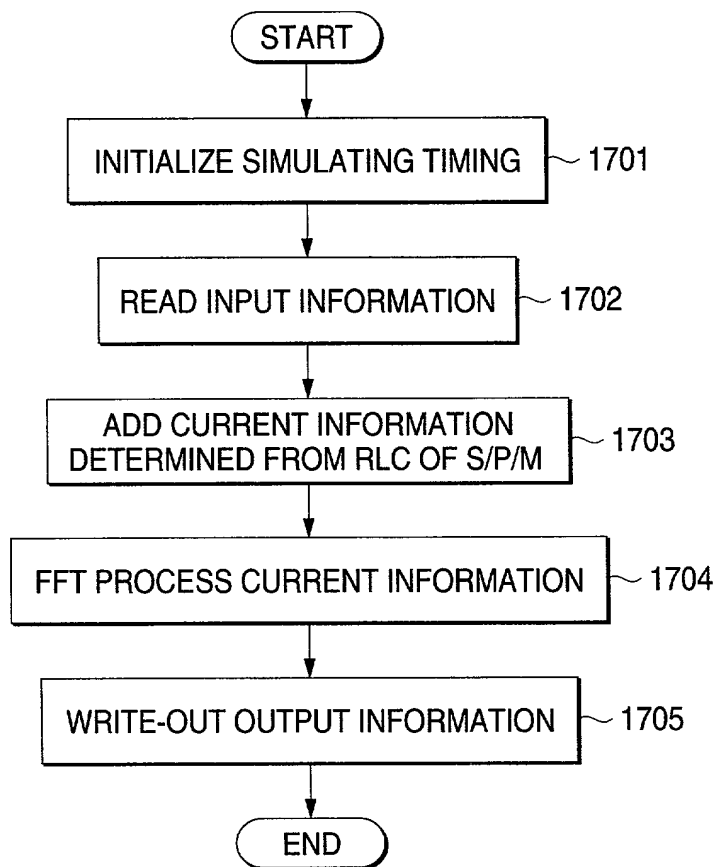


FIG. 18

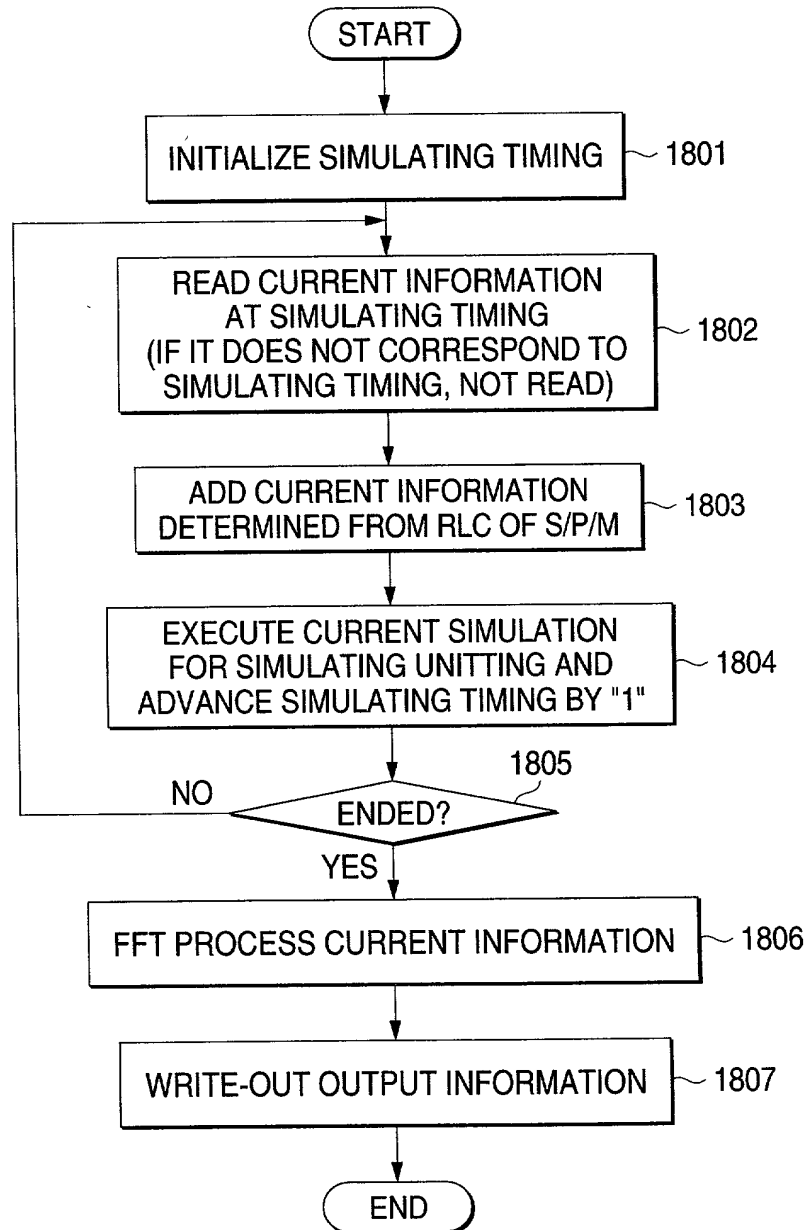


FIG. 19

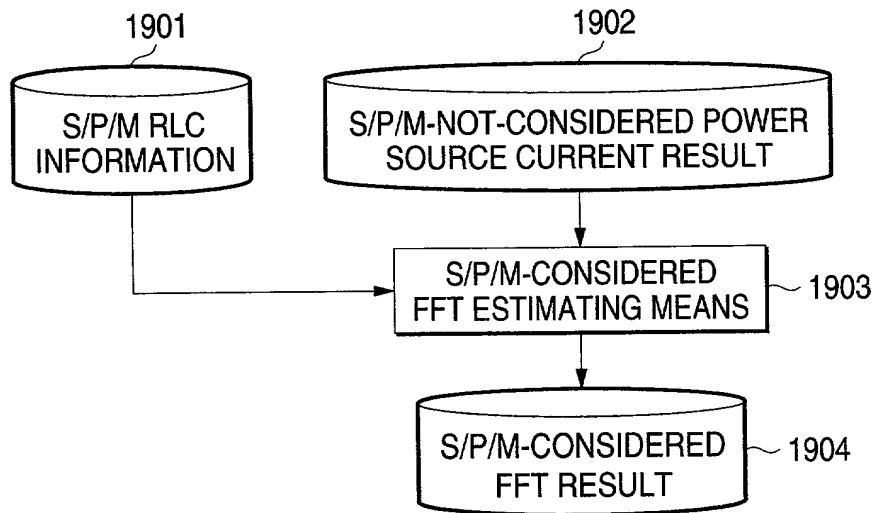


FIG. 20

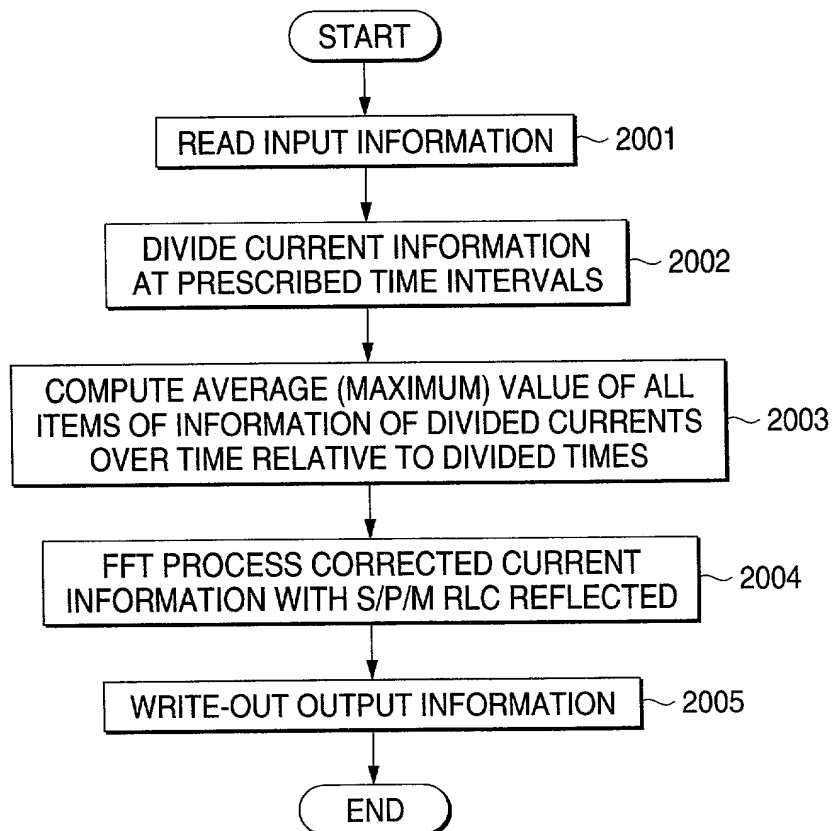


FIG. 21

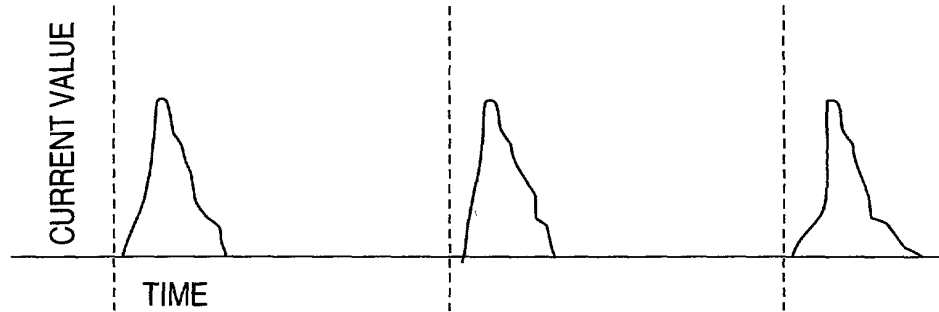


FIG. 22

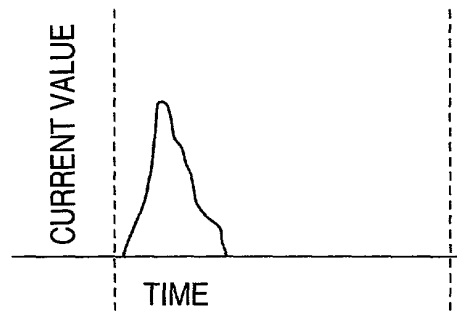


FIG. 23

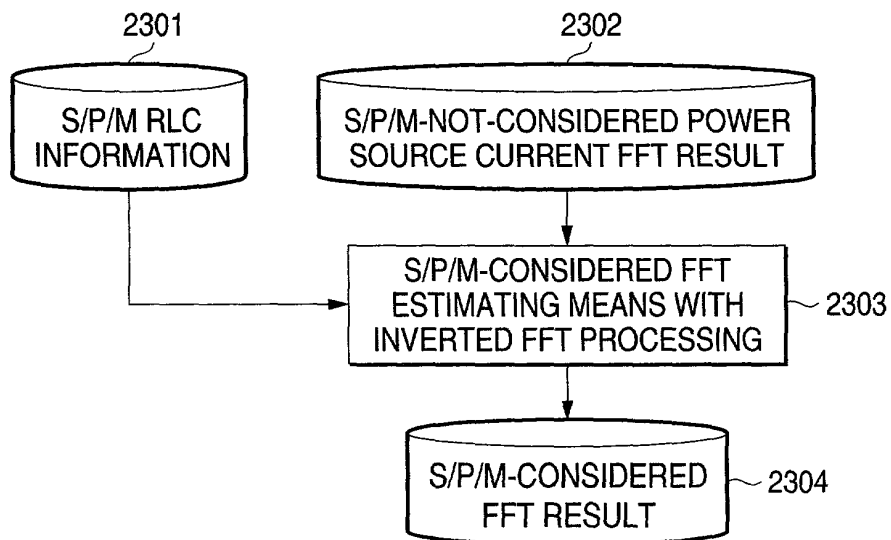


FIG. 24

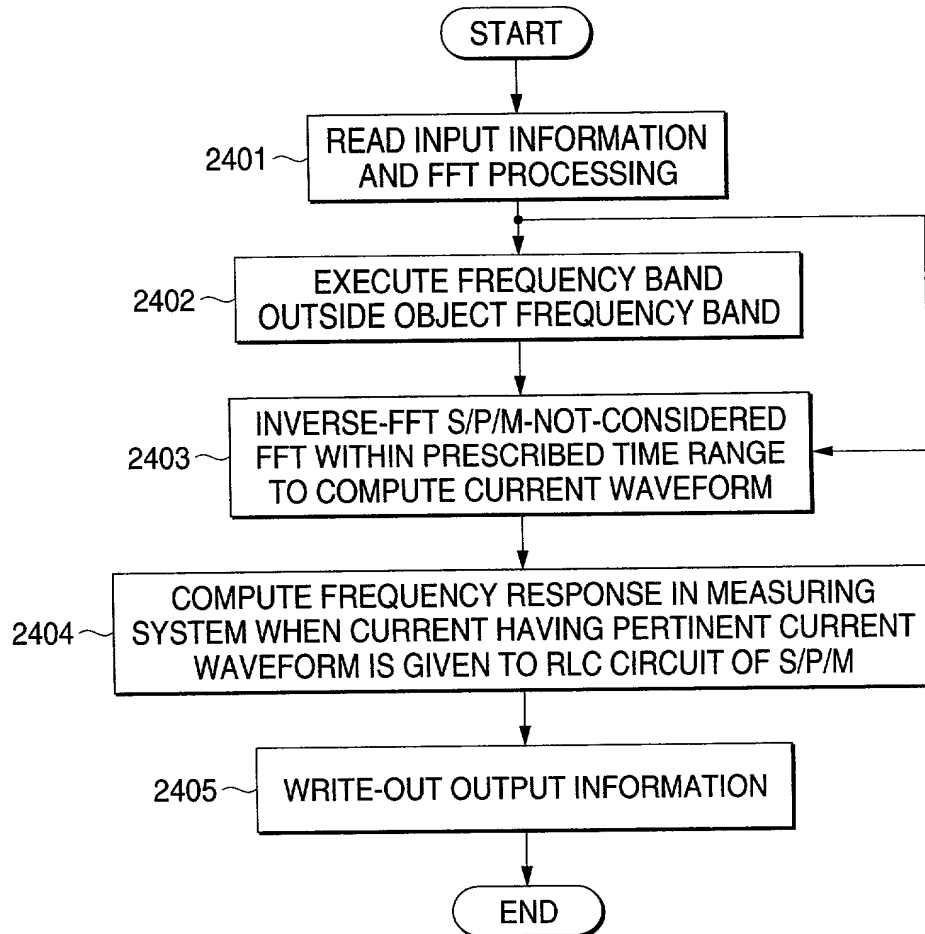


FIG. 25

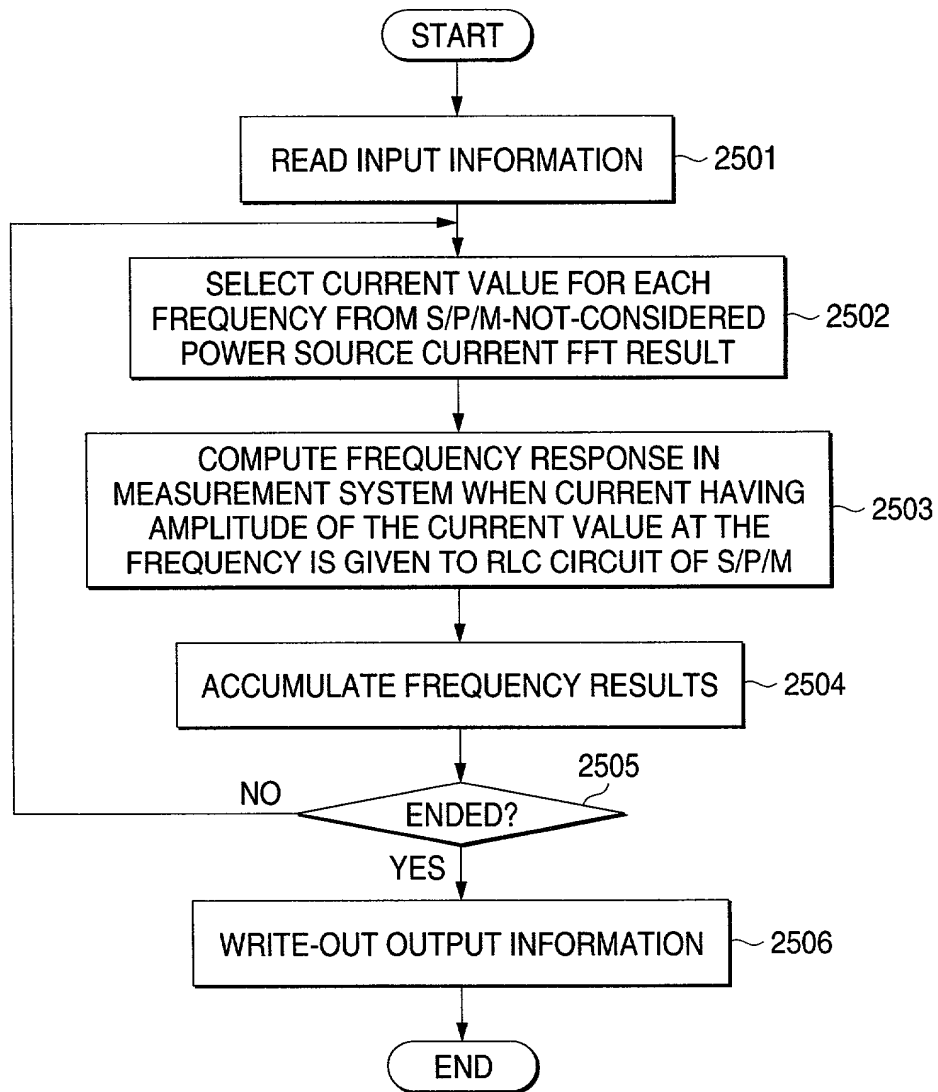




FIG. 26

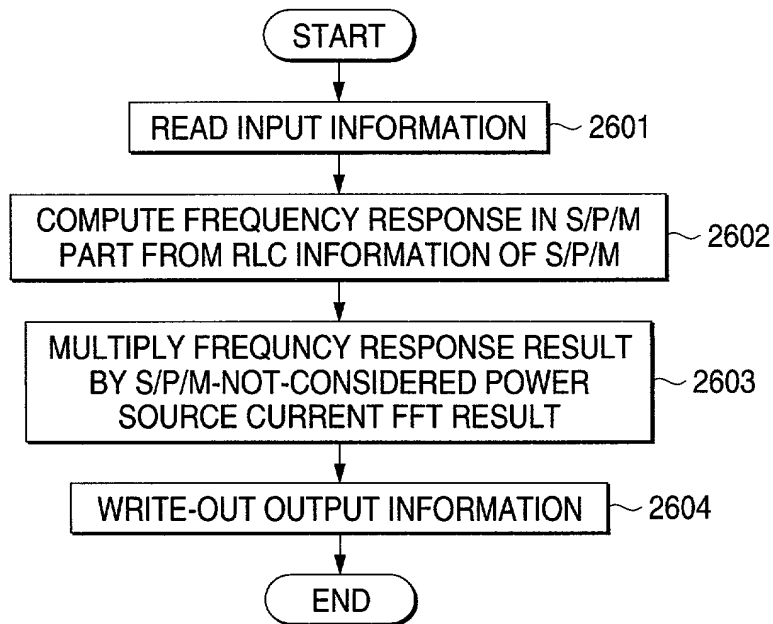


FIG. 27

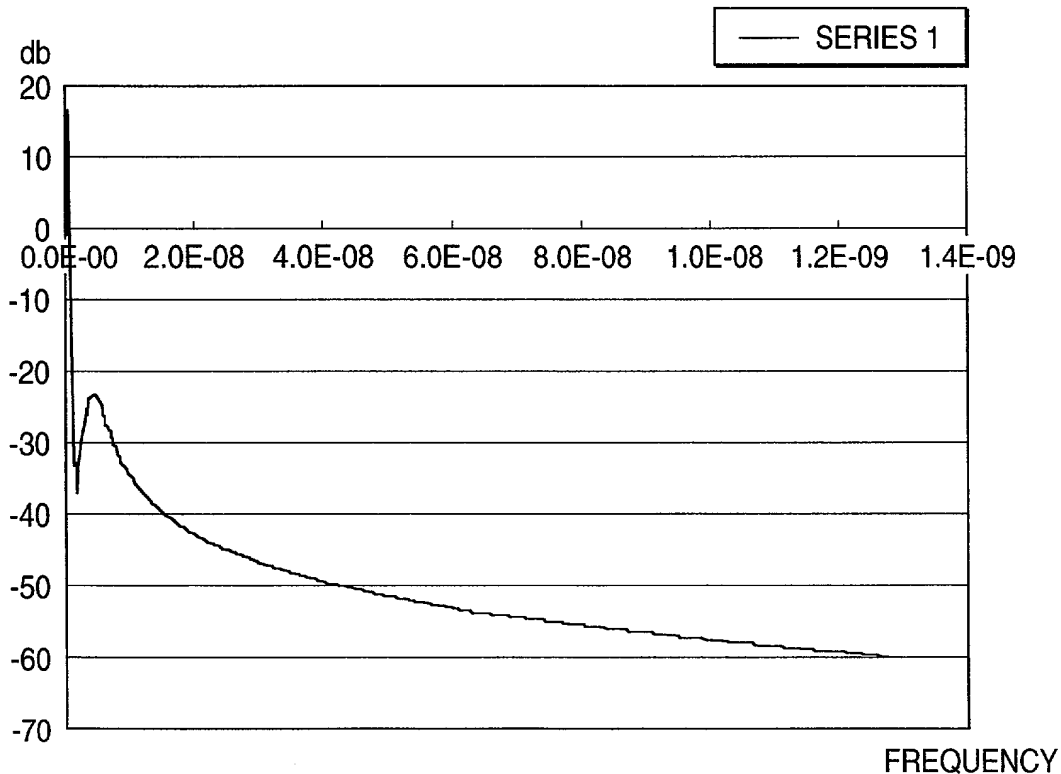


FIG. 28

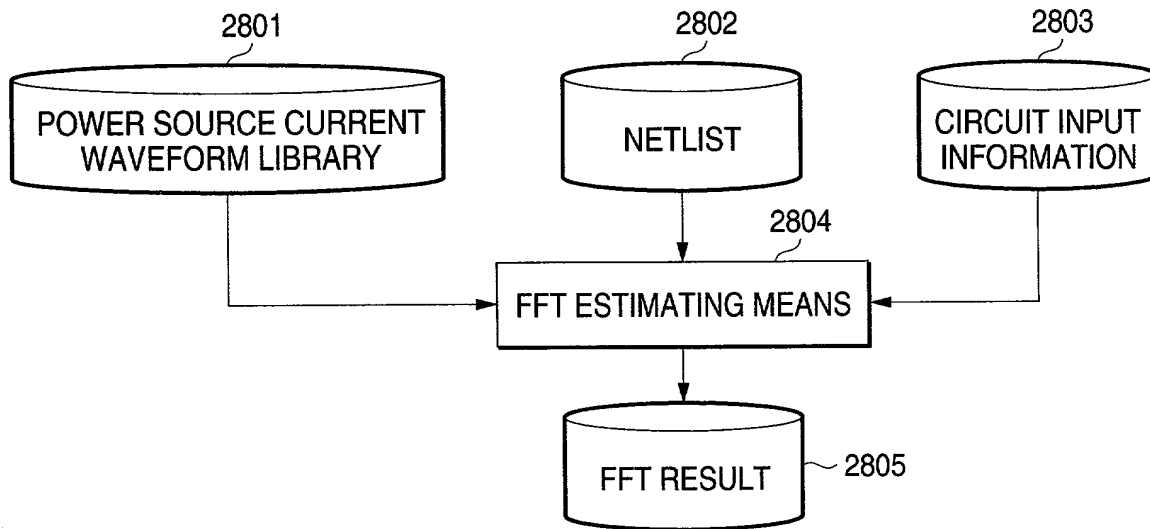


FIG. 29

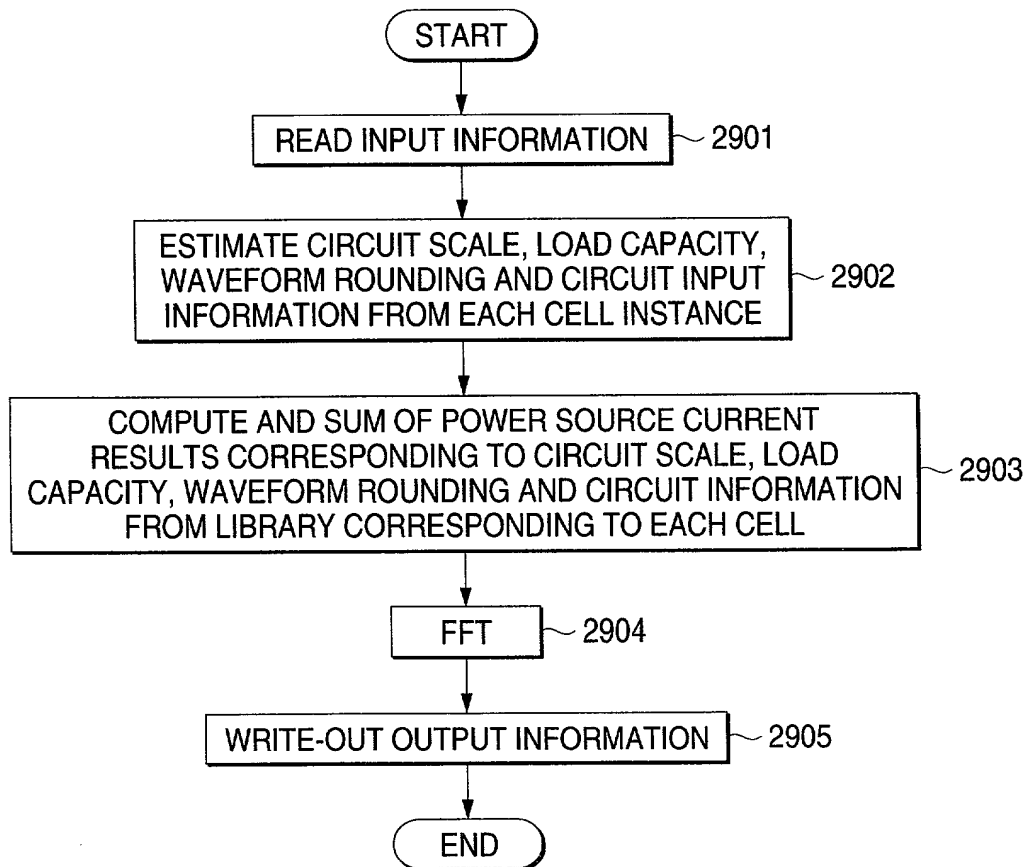


FIG. 30

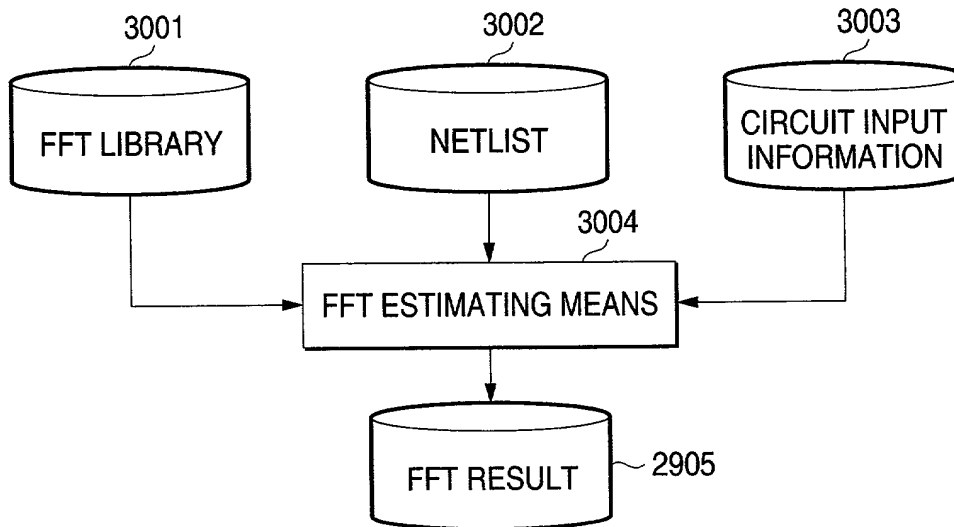


FIG. 31

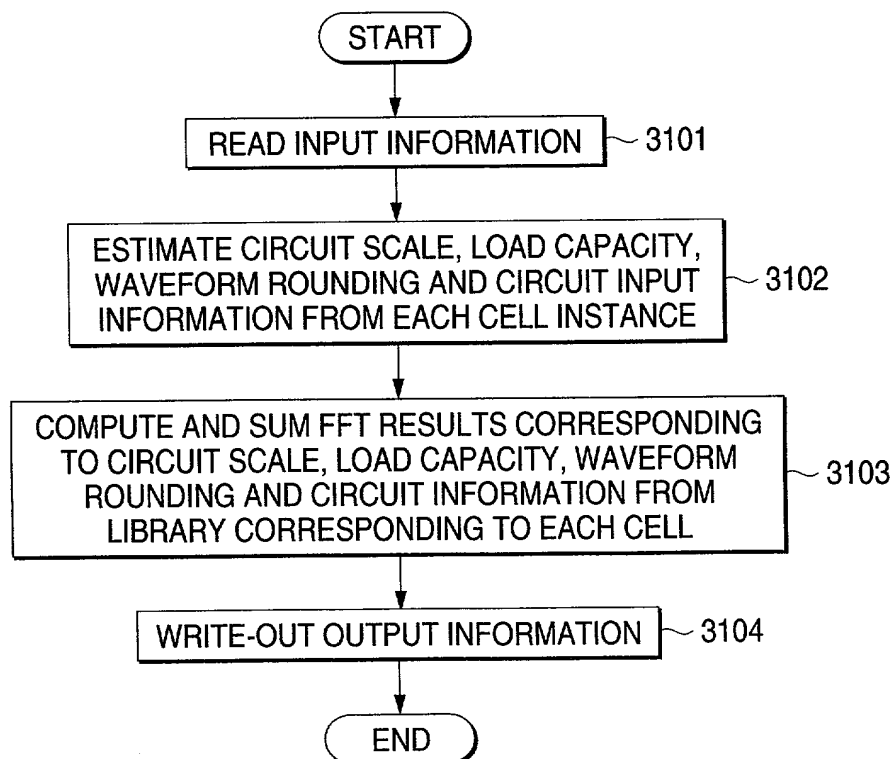


FIG. 32

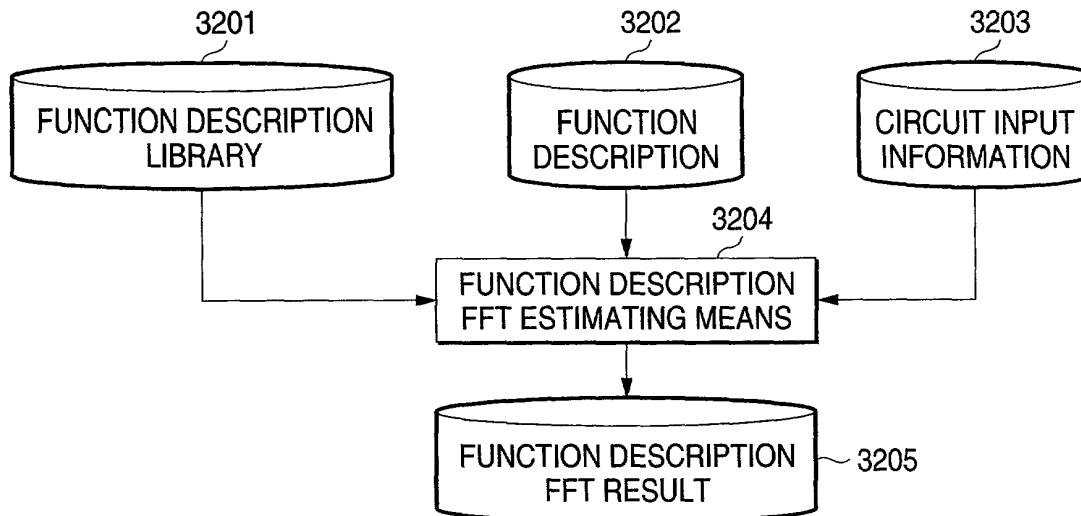


FIG. 33

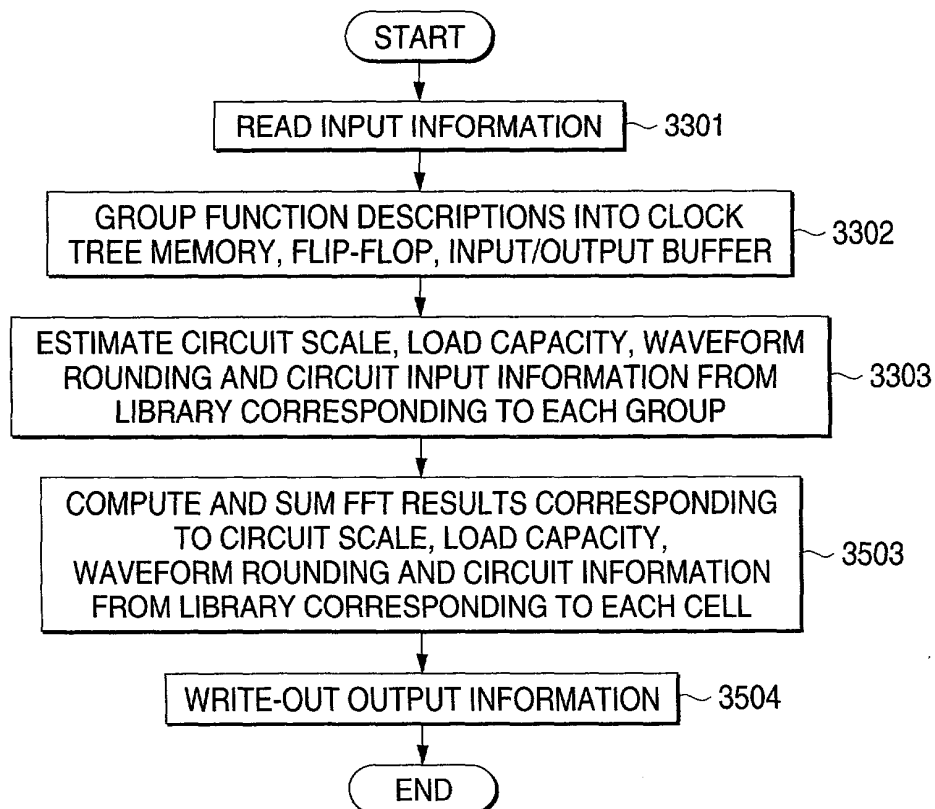


FIG. 34

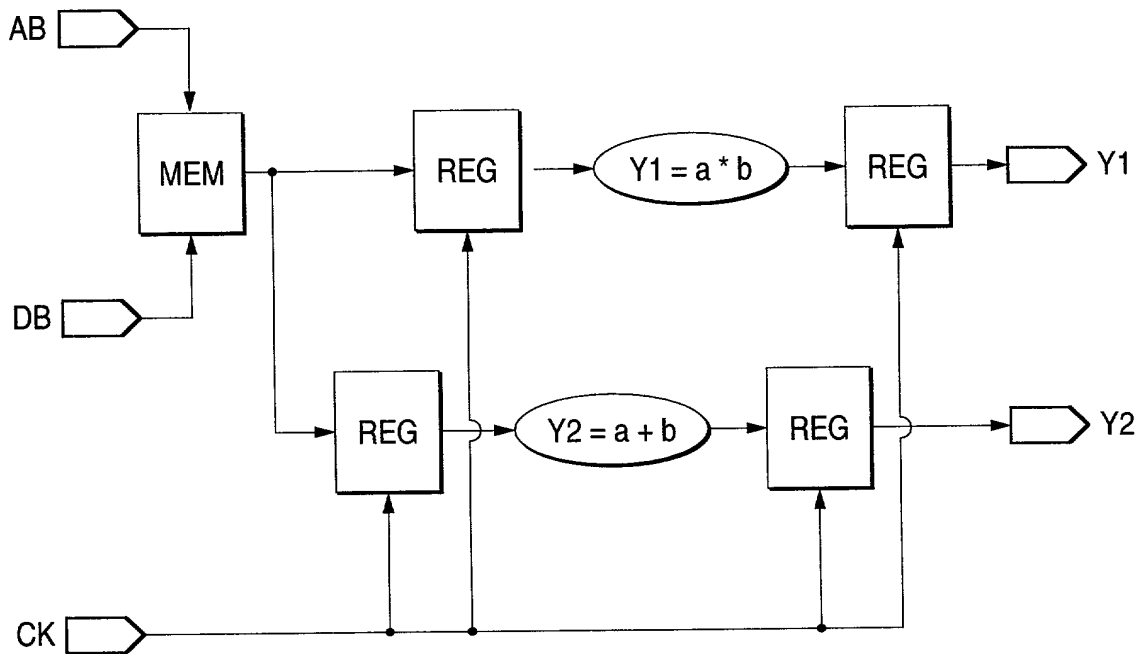


FIG. 35

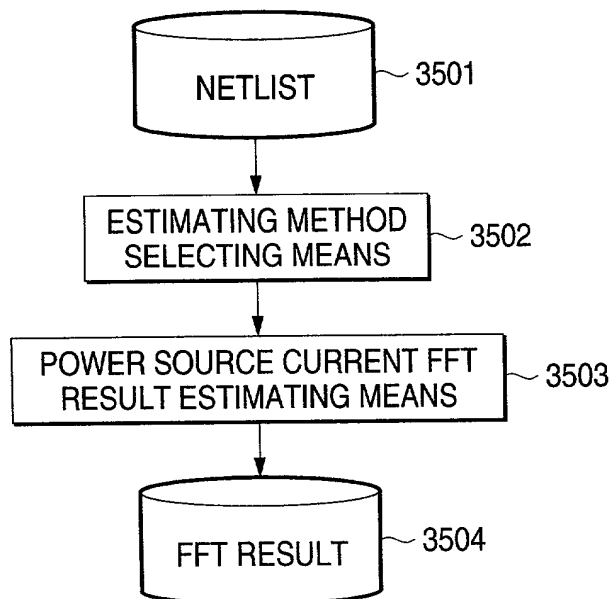


FIG. 36

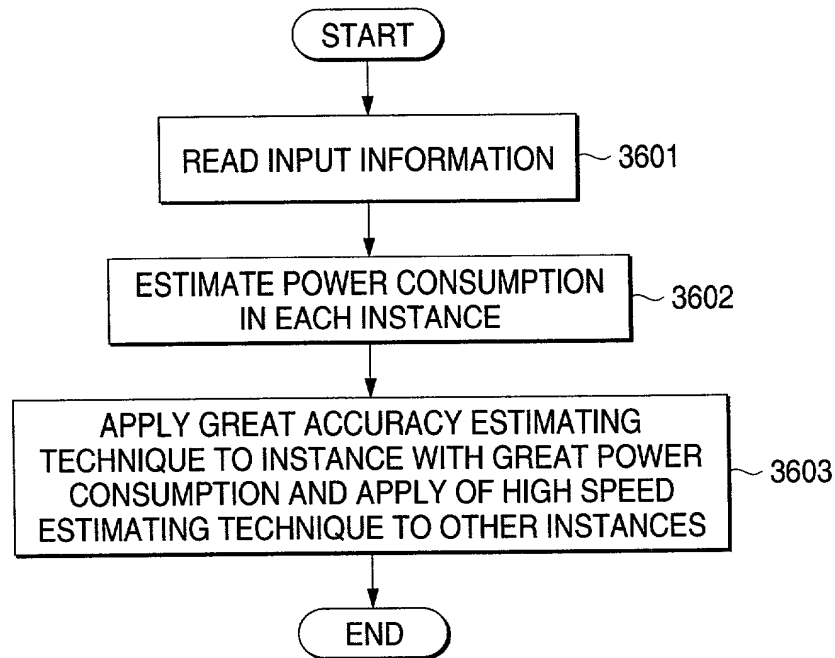


FIG. 37

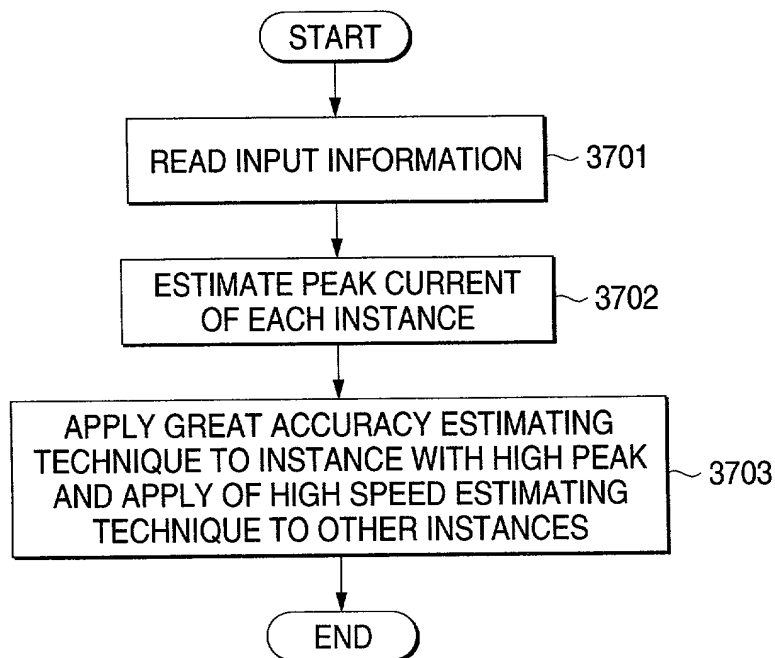


FIG. 38

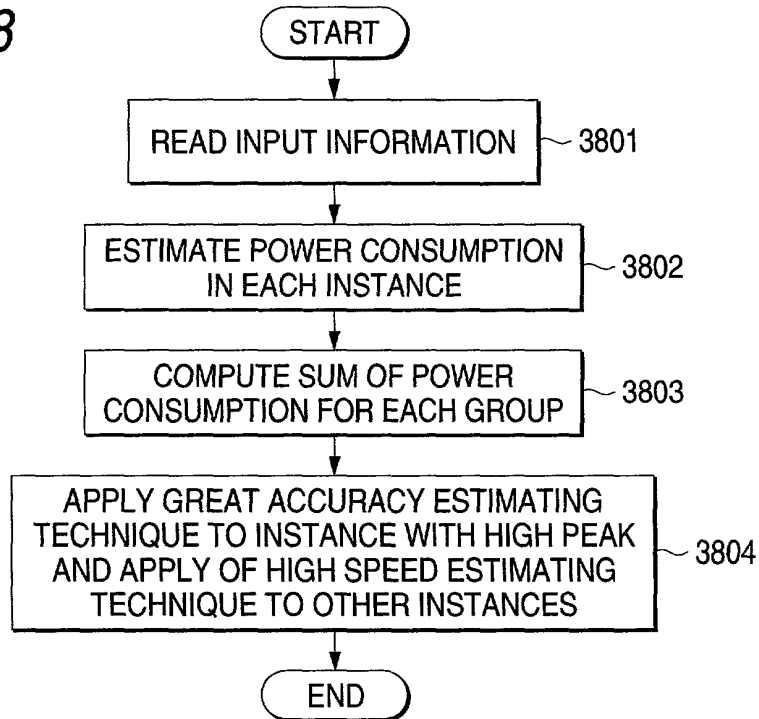


FIG. 39

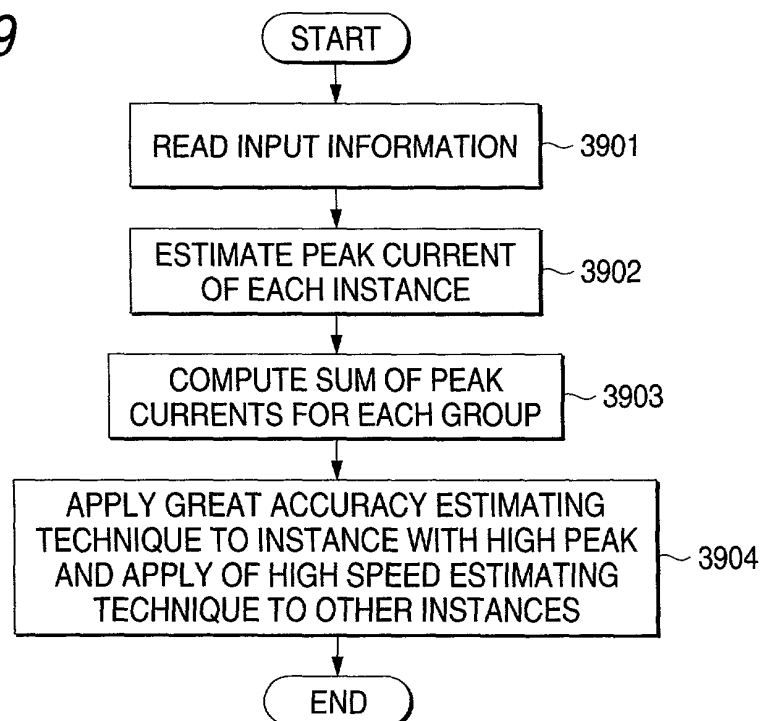


FIG. 40

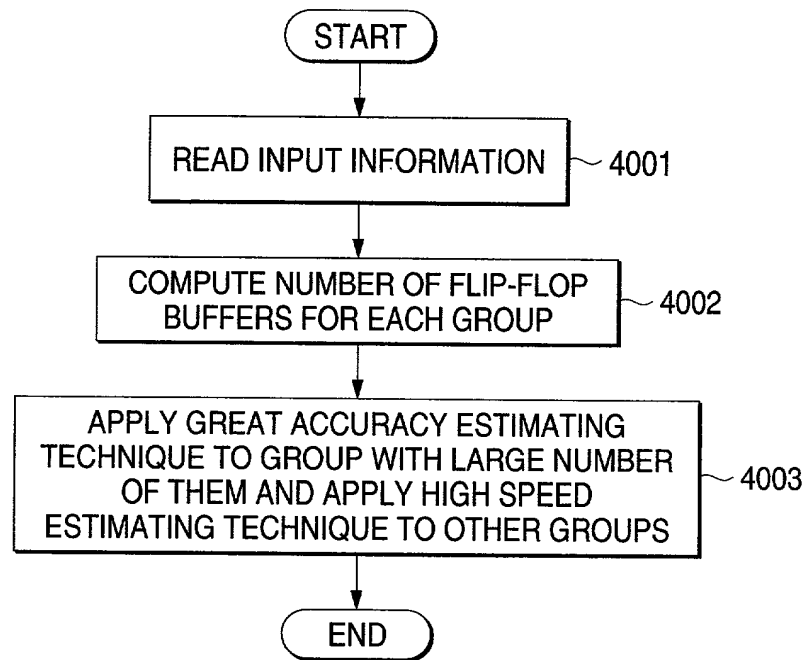
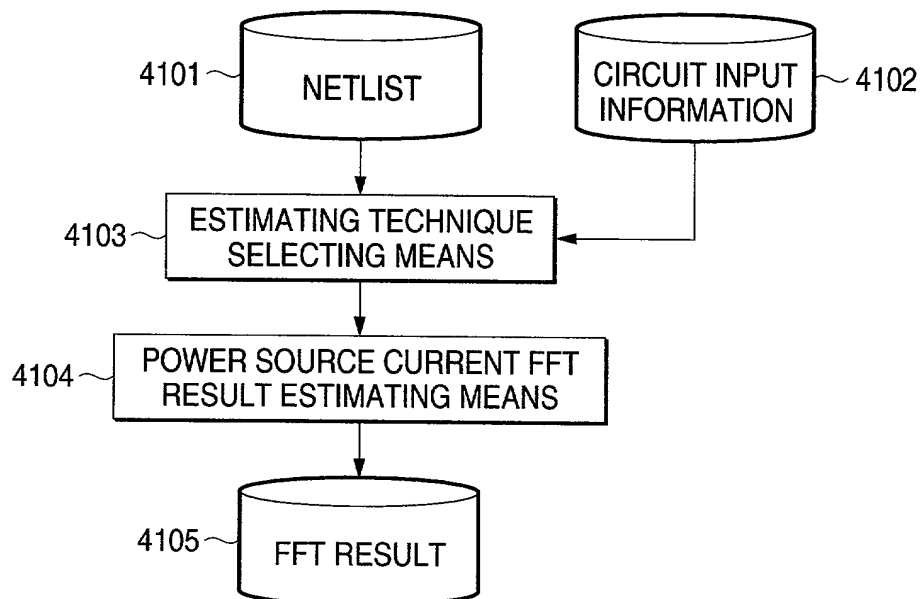


FIG. 41





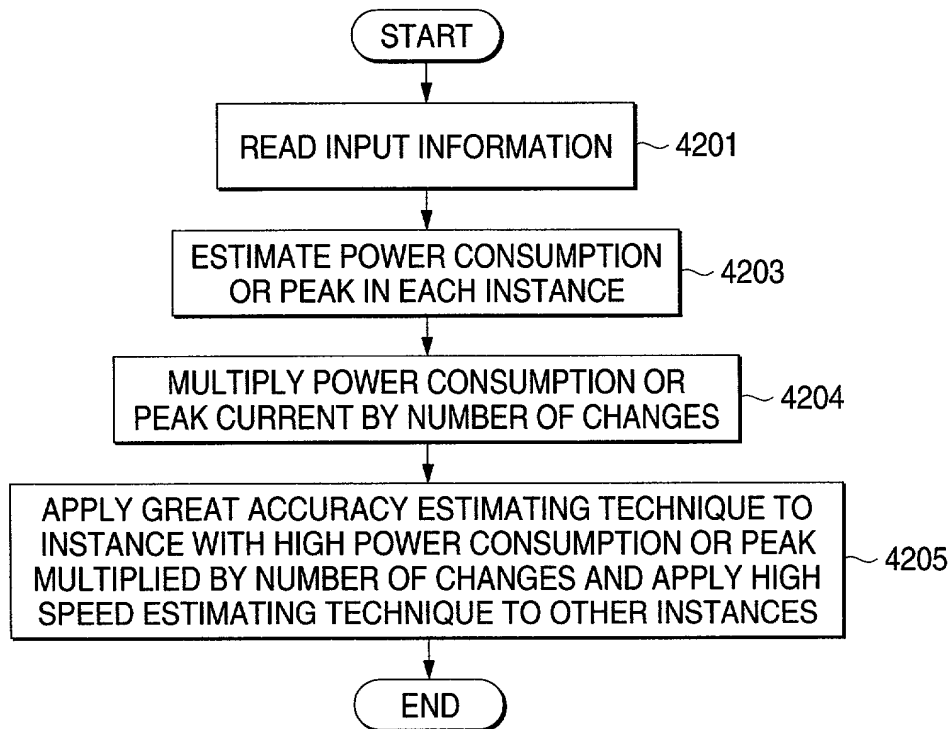
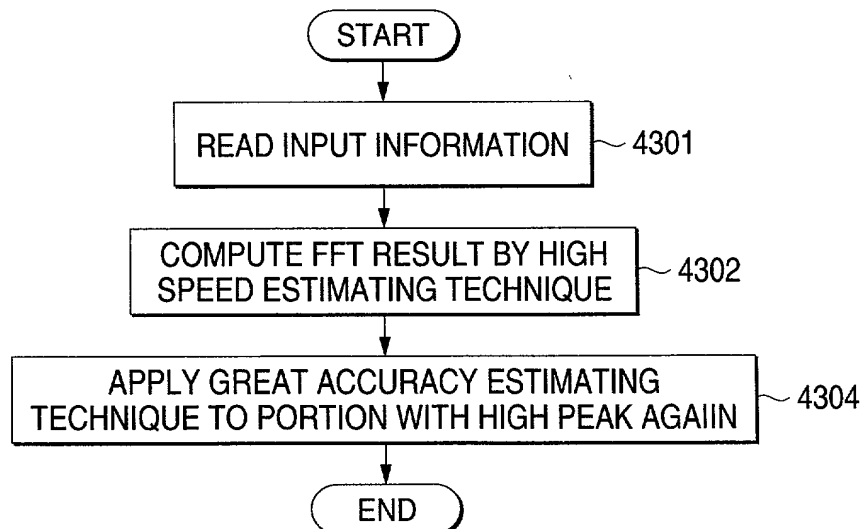
*FIG. 42**FIG. 43*

FIG. 44

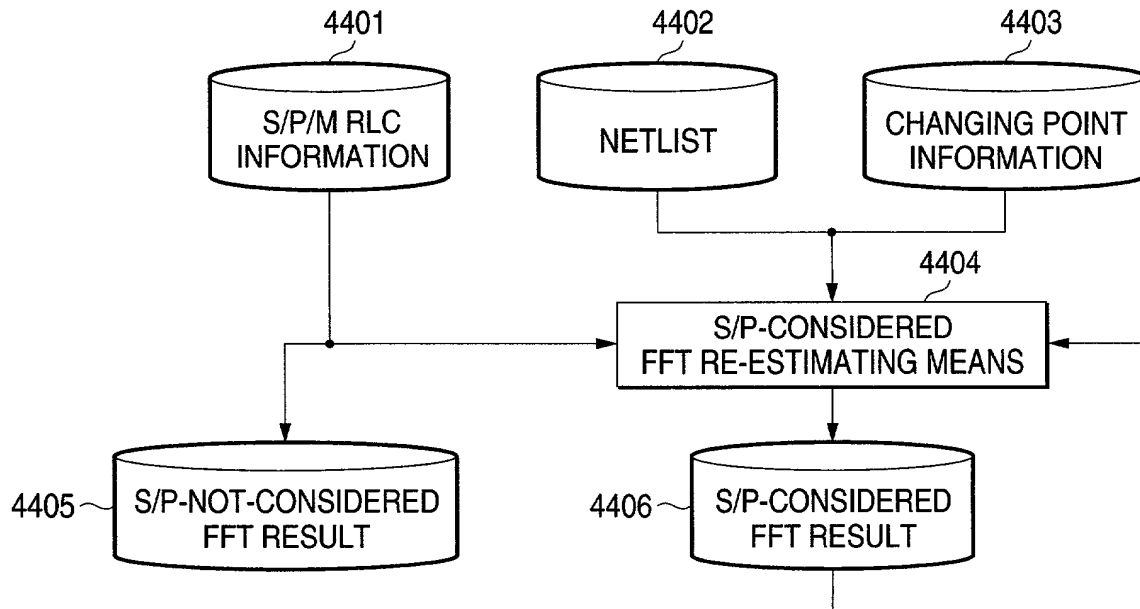


FIG. 45

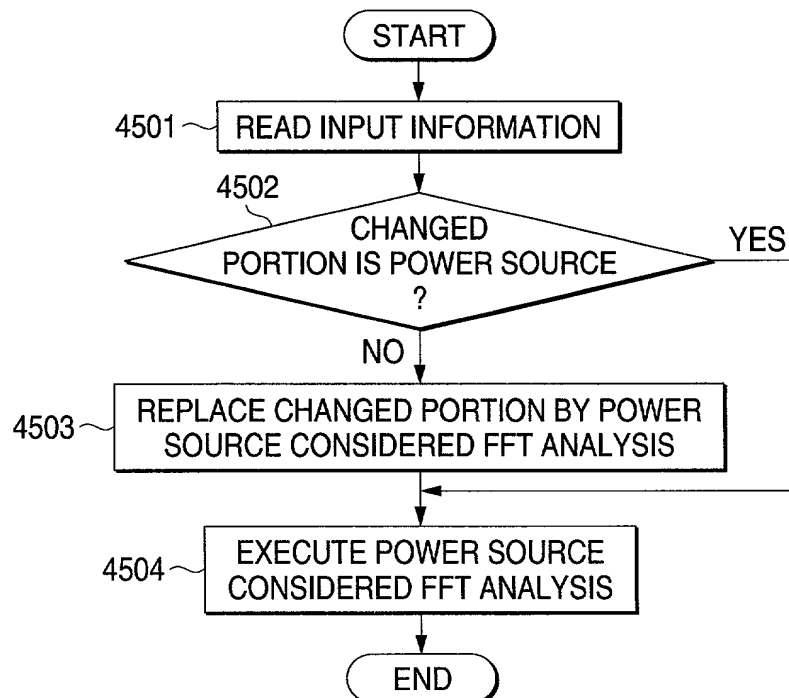


FIG. 46

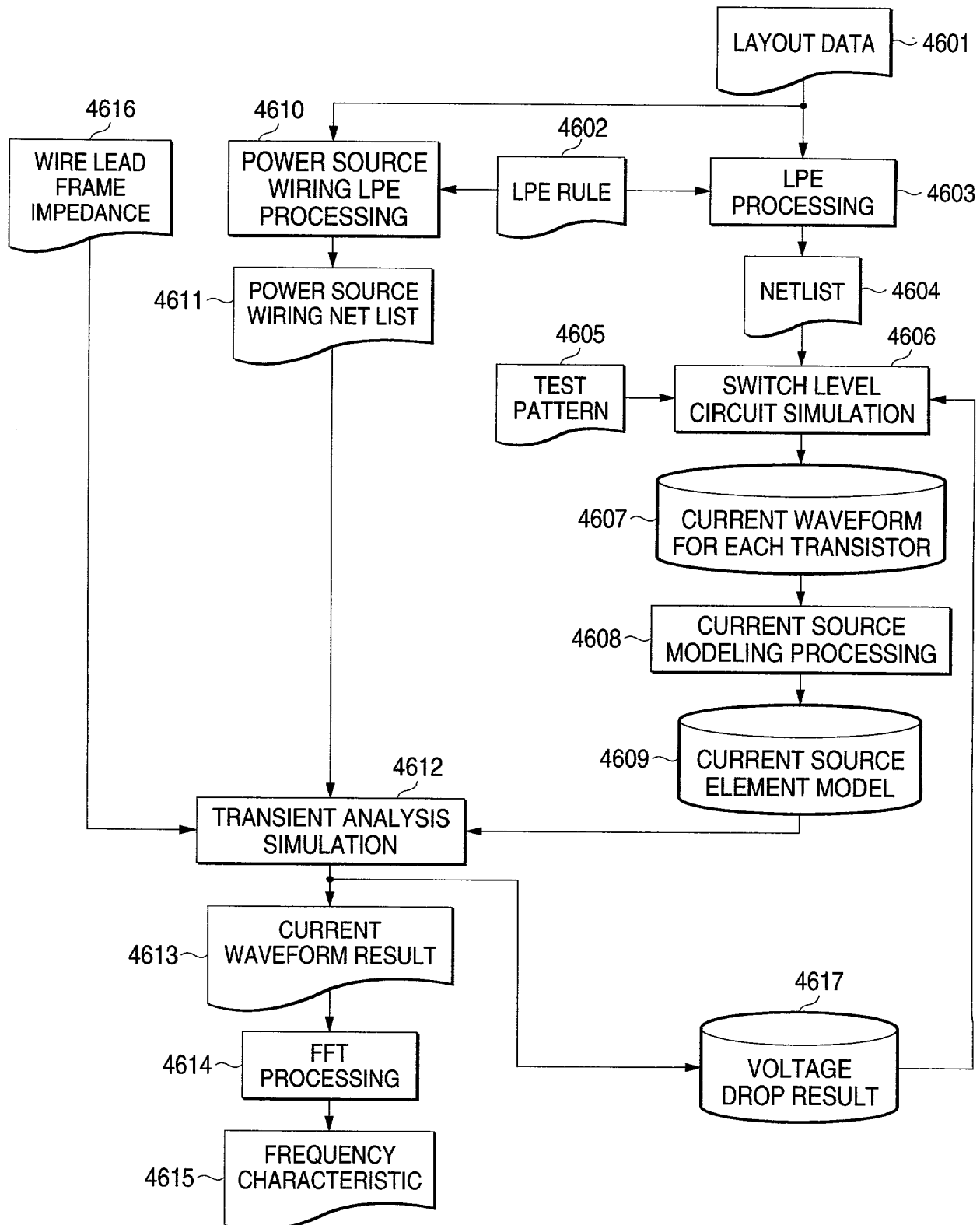


FIG. 47

